Docket No. AUS920030554US1

ABSTRACT OF THE DISCLOSURE

METHOD AND APPARATUS FOR IDENTIFYING
FALSE CACHE LINE SHARING

A method, apparatus, and computer instructions in a
data processing system for processing instructions are
provided. Instructions are received at a processor in
the data processing system. If a selected indicator is
associated with the instruction, counting of each event
associated with the execution of the instruction is
enabled. In some embodiments, the performance indicators
may be utilized to obtain information regarding the
nature of the cache hits and reloads of cache lines
within the instruction or data cache. These embodiments
may be used to determine whether processors of a
multiprocessor system, such as a symmetric multiprocessor
(SMP) system, are truly sharing a cache line or if there
is false sharing of a cache line. This determination may
then be used as a means for determining how to better
store the instructions/data of the cache line to prevent
false sharing of the cache line.